METHODS AND CIRCUITS FOR TESTING PROGRAMMABILITY OF A SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A BREAKDOWN PHENOMENA IN AN ULTRA-THIN DIELECTRIC

ABSTRACT OF THE DISCLOSURE

A method of testing the programmability of a memory cell is disclosed. The memory cell comprises a select transistor and a data storage element. The method comprises applying a test voltage across the data storage element. The select transistor is turned on. Finally, a current flow through the data storage element when the test voltage is applied is measured. A test positive signal is indicated if the current flow is greater than a reference.